WHAT IS CLAIMED IS:

1. A multi-level circuit substrate comprising:

at least two interconnect layers oppositely placed to each other;

an insulator provided between said interconnect layers;

connection members provided penetrating through said insulator along an opposed direction of said interconnect layers and connecting between said interconnect layers;

an intermediate connection layer sandwiched by said connection members at a center position of said connection members provided along the opposed direction of said interconnect layers and electrically connecting between one end and the other end of said connection members;

a shield layer provided nearly on a same plane as said intermediate connection layer and placed spaced from around said intermediate connection layer; and

wherein a condition of $(R \cdot r)/(2 \cdot h) \leq L \leq (5 \cdot R \cdot r)/h$ is satisfied, provided that a connection distance between said interconnect layers through said connection members and said intermediate connection layer is h, said connection members where considered generally as a circular cylinder has a diameter R, said intermediate connection layer where considered generally as circular has a diameter r, and a spaced distance between said intermediate connection layer and said shield layer is L.

2. A multi-level circuit substrate according to claim 1, wherein said insulator has lower and upper insulation layers placed stacked with each other, said intermediate connection layer and aid shield layer being sandwiched between said lower insulation layer and said upper insulation layer; and

said connection members comprising:

a lower connection member provided penetrating through said lower insulation layer in a thickness direction thereof and electrically connecting between said interconnect layer positioned lower and said intermediate connection layer; and

an upper connection member provided penetrating through said upper insulation layer in a thickness direction thereof and electrically connecting between said interconnect layer positioned upper and said intermediate connection layer.

3. A multi-level circuit substrate according to claim 1, wherein said shield layer is a ground layer.

4. A multi-level circuit substrate according to claim 1, wherein said shield layer is a power source layer.

5. A multi-level circuit substrate according to claim 1, wherein said multi-level circuit substrate transmits a signal having a wavelength of shorter than 1500 times said connection distance h.

6. A multi-level circuit substrate comprising:

at least two interconnect layers oppositely placed to each other;

a first insulator provided between said interconnect layers;

connection members provided penetrating through said first insulator along an opposed direction of said interconnect layers and connecting between said interconnect layers;

an intermediate connection layer sandwiched by said connection members at a center position of said connection members provided along the opposed direction of said interconnect layers and electrically connecting between one end and the other end of said connection members;

a shield layer provided nearly on a same plane as said intermediate connection layer and placed spaced from around said intermediate connection layer; and

wherein a gap formed between said intermediate connection layer and said shield layer is filled by a second insulator having a lower specific dielectric constant than said first insulator.

7. A multi-level circuit substrate according to claim 6, wherein a condition of $(R \cdot r \cdot \sqrt{\varepsilon'})/(2 \cdot h \cdot \sqrt{\varepsilon}) \leq L \leq (5 \cdot R \cdot r \cdot \sqrt{\varepsilon'})/(h \cdot \sqrt{\varepsilon})$ is satisfied, provided that a specific dielectric constant of said first insulator is ε, a specific dielectric constant of said second insulator is ε', a connection distance between said interconnect layers through said connection members and said intermediate connection layer is h, said connection members where considered generally as a

circular cylinder has a diameter R, said intermediate connection layer where considered generally as circular has a diameter r, and a spaced distance between said intermediate connection layer and said shield layer is L.

8. A multi-level circuit substrate according to claim 6, wherein said first insulator has lower and upper insulation layers placed stacked with each other;

said intermediate connection layer and aid shield layer being sandwiched between said lower insulation layer and said upper insulation layer; and

said connection members comprising:

a lower connection member provided penetrating through said lower insulation layer in a thickness direction thereof and electrically connecting between said interconnect layer positioned lower and said intermediate connection layer; and

an upper connection member provided penetrating through said upper insulation layer in a thickness direction thereof and electrically connecting between said interconnect layer positioned upper and said intermediate connection layer.

9. A multi-level circuit substrate according to claim 6, wherein said shield layer is a ground layer.

10. A multi-level circuit substrate according to claim 6, wherein said shield layer is a power source layer.

11. A multi-level circuit substrate according to claim 6, wherein said multi-level circuit substrate transmits a

signal having a wavelength of shorter than 1500 times said connection distance h.

12. A multi-level circuit substrate comprising:

at least two first shield layers oppositely placed to each other;

an insulator provided between said first shield layers;

at least two interconnect layers placed within said insulator substantially in parallel with said first shield layers and oppositely to each other;

connection members provided penetrating through said insulator along an opposed direction of said interconnect layers and connecting between said interconnect layers;

an intermediate connection layer sandwiched by said connection members at a center position of said connection members provided along the opposed direction of said interconnect layers and electrically connecting between one end and the other end of said connection members;

a second shield layer provided generally on a same plane as said intermediate connection layer and placed spaced from around said intermediate connection layer;

wherein, provided that said interconnect layers where considered generally as circular have a diameter m and said intermediate connection layer where considered generally as circular has a diameter r, $r < m$ is given where said connection

members are high in characteristic impedance than said interconnect layers.

13. A multi-level circuit substrate comprising:

at least two first shield layers oppositely placed to each other;

an insulator provided between said first shield layers;

at least two interconnect layers placed within said insulator substantially in parallel with said first shield layers and oppositely to each other;

connection members provided penetrating through said insulator along an opposed direction of said interconnect layers and connecting between said interconnect layers;

an intermediate connection layer sandwiched by said connection members at a center position of said connection members provided along the opposed direction of said interconnect layers and electrically connecting between one end and the other end of said connection members;

a second shield layer provided generally on a same plane as said intermediate connection layer and placed spaced from around said intermediate connection layer;

wherein, provided that said interconnect layers where considered generally as circular have a diameter m and said intermediate connection layer where considered generally as circular has a diameter r, $r > m$ is given where said connection

members are low in characteristic impedance than said interconnect layers.

14. A method for adjusting a characteristic impedance for a multi-level circuit substrate, said multi-level circuit substrate comprising:

at least two first shield layers oppositely placed to each other;

an insulator provided between said first shield layers;

at least two interconnect layers placed within said insulator substantially in parallel with said first shield layers and oppositely to each other;

connection members provided penetrating through said insulator along an opposed direction of said interconnect layers and connecting between said interconnect layers;

an intermediate connection layer sandwiched by said connection members at a center position of said connection members provided along the opposed direction of said interconnect layers and electrically connecting between one end and the other end of said connection members; and

a shield layer provided generally on a same plane as said intermediate connection layer and placed spaced from around said intermediate connection layer;

wherein, provided that said interconnect layers where considered generally as circular have a diameter m and said intermediate connection layer where considered generally as

circular has a diameter r, r < m is given where said connection members are high in characteristic impedance than said interconnect layers, and

Wherein, r > m is given where said connection members are low in characteristic impedance than said interconnect layers.

15. A method for manufacturing a multi-level circuit substrate, comprising:

a step of forming a lower interconnect layer on an underside of a lower insulation layer, and a lower connection member inside of and penetrating through said lower insulation layer in a thickness direction thereof and electrically connected with said lower interconnect layer;

a step of forming an intermediate connection layer electrically connected with said lower interconnect layer on an upper surface of said lower insulation layer, and a shield layer placed spaced from around said intermediate connection layer;

a step of forming a coat layer on said upper surface of said lower insulation layer, and forming in said coat layer an opening substantially coincident with a gap between said intermediate connection layer and said lower interconnect layer;

a step of forming an insulator lower in specific dielectric constant than said lower insulation layer, and

removing said insulator together with said coat layer except for said insulator on said opening;

a step of forming an upper insulation layer equivalent in specific dielectric constant to said lower insulation layer on said upper surface of said lower insulation layer;

a step of forming an upper connection member inside of and penetrating through said lower insulation layer in a thickness direction thereof and electrically connected with said intermediate connection layer; and

a step of forming an upper interconnect layer electrically connected with said upper connection member on an upper surface of said upper insulation layer.